

PREPARED BY:	DATE
APPROVED BY:	DATE

# SHARP

INTEGRATED CIRCUITS GROUP  
SHARP CORPORATION

## SPECIFICATION

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REPRESENTATIVE DEPARTMENT

DEVICE SPECIFICATION FOR

16K CMOS STATIC RAM (2,048 X 8bit)

MODEL No.

LH5116NA-10

CUSTOMERS APPROVAL

DATE


\_\_\_\_\_

BY

\_\_\_\_\_

PRESENTED

BY



H. Kitamori  
Dept. General Manager  
Engineering Dept. 4  
IC Engineerring Center  
Integrated Circuits Group  
SHARP CORPORATION

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**1. General Description**

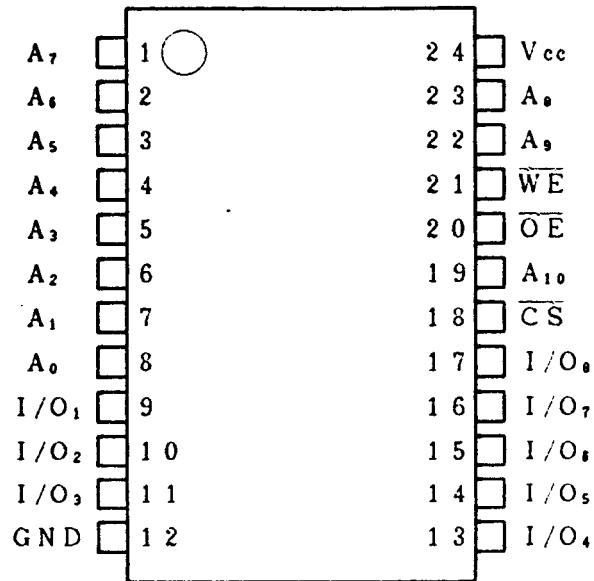
The LH5116NA-10 is a static RAM organized as 16,384(2,048 word x 8bit) fabricated with a CMOS silicon gate process.

It's main features include:

**Features**

- Access time (MAX.) and dissipation current (MAX.)  
100 ns / 40 mA
- Single 5 V power supply (5 V ± 10%)
- Full static operation requiring no clock and refresh cycle
- All input and output TTL compatible
- Three state output
- Pin configuration is compatible with industry standard  
16K EPROM/MASK ROM
- Standard 24-pin Small-Outline Package (SOP)

### 2. Pin Configuration

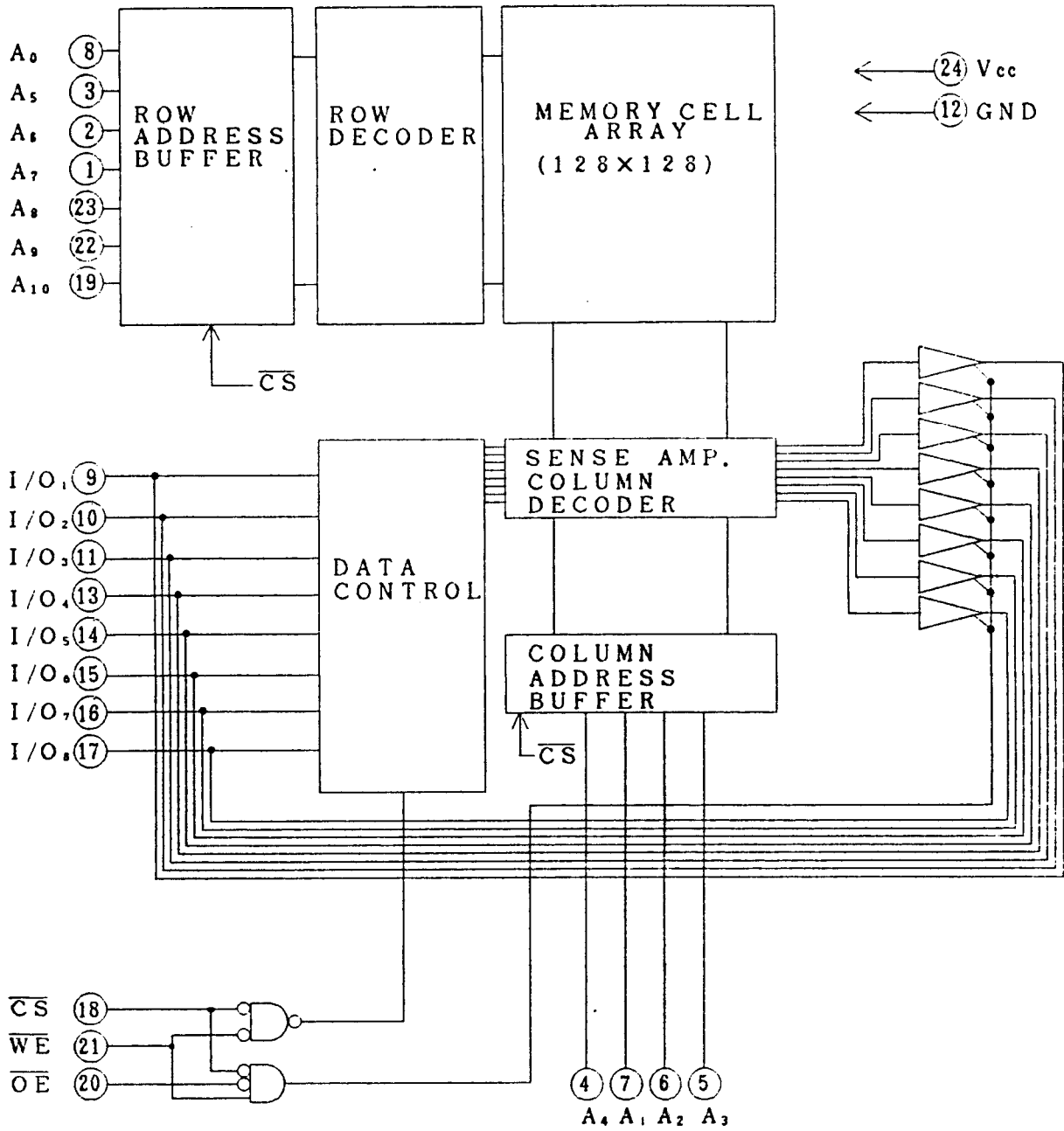


Pin name	Signal
A <sub>0</sub> ~ A <sub>10</sub>	Address input
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
I/O <sub>1</sub> ~ I/O <sub>8</sub>	Data input/output
V <sub>CC</sub>	Power supply
GND	Ground

### 3. Operating Mode

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O <sub>1</sub> ~ I/O <sub>8</sub>	Supply current
H	X	X	Deselect	High impedance	Standby (I <sub>ccL</sub> )
L	L	X	Write	Data input	Operating(I <sub>cc</sub> )
L	H	L	Read	Data output	Operating(I <sub>cc</sub> )
L	X	H	Output disable	High impedance	Operating(I <sub>cc</sub> )

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.3~+7.0	V
Input voltage	V <sub>IN</sub>	-0.3~V <sub>CC</sub> +0.3	V
Operating temperature	T <sub>opr</sub>	0~+70	°C
Storage temperature	T <sub>str</sub>	-55~+150	°C

## 6. DC Electrical Characteristics

V<sub>CC</sub>=5V±10%, T<sub>a</sub>=0~+70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input "LOW" voltage	V <sub>IL</sub>		-0.3		0.8	V
Input "HIGH" voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> +0.3	V
Output "LOW" voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA			0.4	V
Output "HIGH" voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4			V
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =0~V <sub>CC</sub>			1.0	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS} = V_{IH}, V_{I/O} = 0V \sim V_{CC}$			1.0	μA
Dissipation current 1	I <sub>CC1</sub>	$\overline{CS} = 0V$ , other input is 0V~V <sub>CC</sub> , I <sub>I/O</sub> =0mA, ( $\overline{OE} = V_{CC}$ )		2.5	3.0	mA
Dissipation current 2	I <sub>CC2</sub>	$\overline{CS} = V_{IL}$ , other input is V <sub>IL</sub> ~V <sub>IH</sub> , I <sub>I/O</sub> =0mA, ( $\overline{OE} = V_{IH}$ )		3.0	4.0	mA
Standby Dissipation current	I <sub>CCL</sub>	$\overline{CS} \geq V_{CC} - 0.2V$ other input is 0V~V <sub>CC</sub>			1.0	μA
					0.2*	μA

Note)\* T<sub>a</sub>=25°C

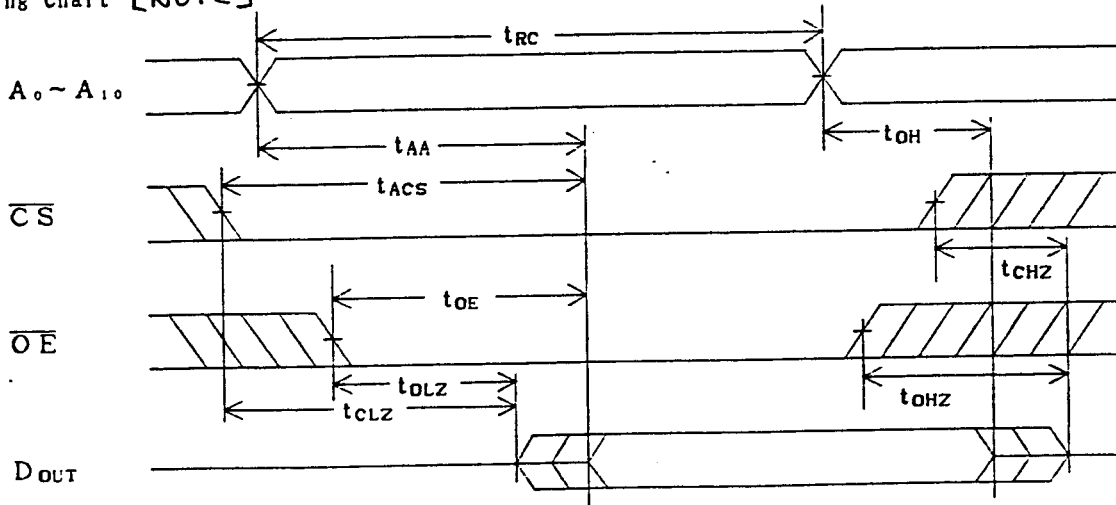
7. AC Characteristics

Read cycle

$V_{CC} = 5V \pm 10\%$ ,  $T_a = 0 \sim +70^\circ C$

Parameter	Symbol	MIN	MAX	Unit
Read cycle time	$t_{RC}$	100		ns
Address access time	$t_{AA}$		100	ns
Chip enable access time	$t_{ACS}$		100	ns
Output floating hold time with respect to chip select	$t_{CLZ}$	10		ns
Output enable access time	$t_{OE}$		40	ns
Output floating hold time with respect to output enable	$t_{OLZ}$	10		ns
Output floating time with respect to chip select	$t_{CHZ}$	0	40	ns
Output floating time with respect to output enable	$t_{OHZ}$	0	40	ns
Previous read data valid with respect to address change	$t_{OH}$	10		ns

Timing Chart [NOTE]



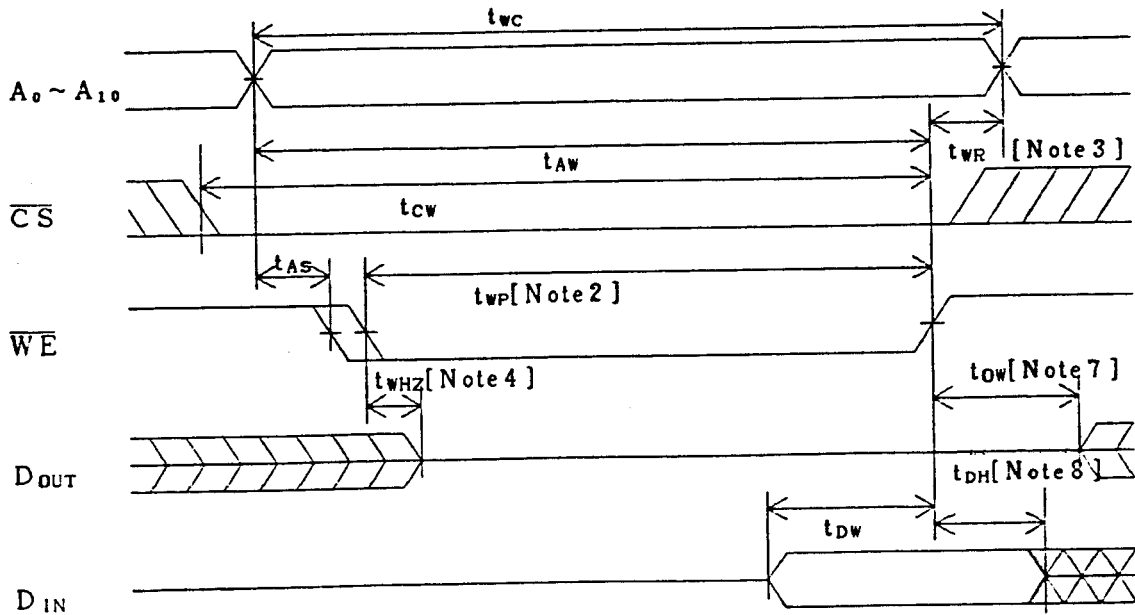
Note)  $\overline{WE}$  is "High" level during the read cycle

Write Cycle

$V_{CC} = 5V \pm 10\%$ ,  $T_a = 0 \sim +70^\circ C$

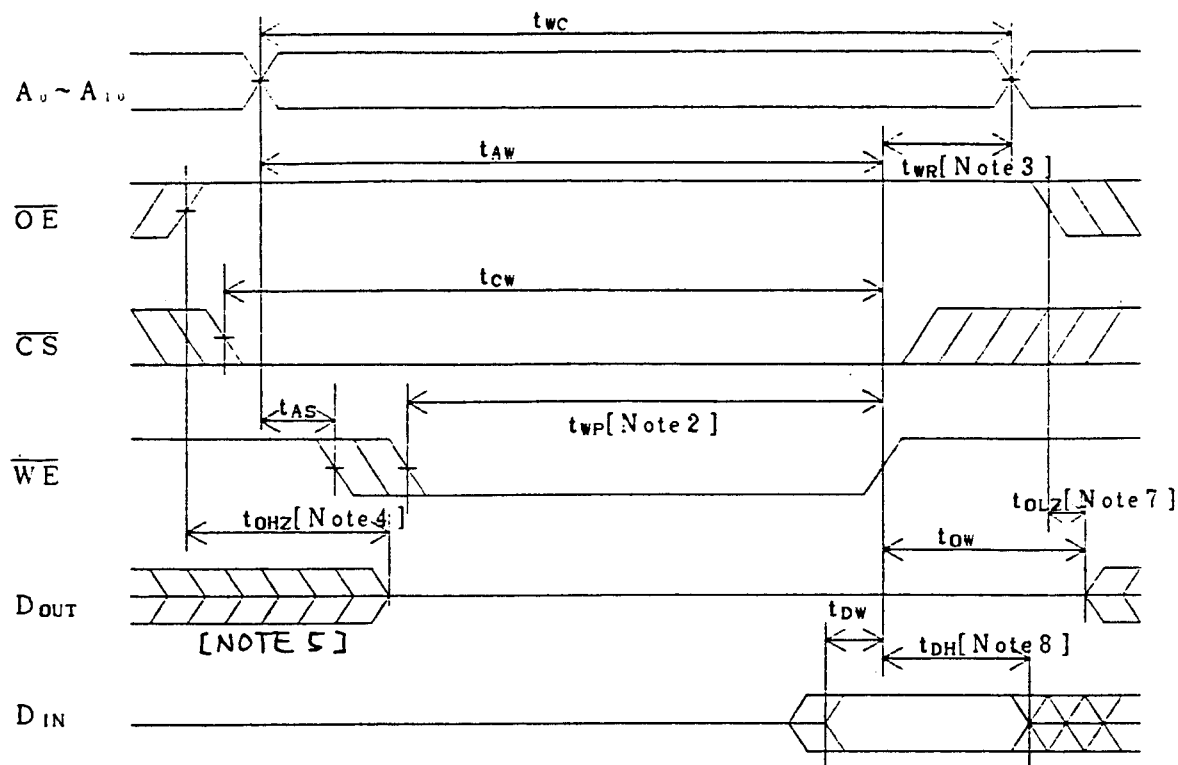
Parameter	Symbol	MIN	MAX	Unit
Write cycle	t <sub>wc</sub>	100		ns
Chip enable to write	t <sub>cw</sub>	80		ns
Write delay	t <sub>AW</sub>	80		ns
Address setup time	t <sub>AS</sub>	0		ns
Write pulse width	t <sub>WP</sub>	60		ns
Write recovery	t <sub>WR</sub>	10		ns
Output floating time with respect to write pulse	t <sub>WHZ</sub>		30	ns
Data setup time	t <sub>DW</sub>	30		ns
Data hold time	t <sub>DH</sub>	10		ns
Output floating time with respect to write	t <sub>OW</sub>	10		ns
Output hold time with respect to output enable	t <sub>OHZ</sub>		40	ns

Timing Chart(No.1)[Note1,6]





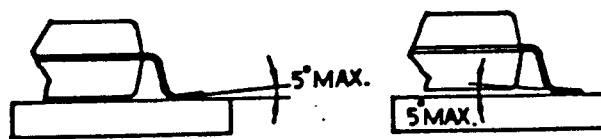
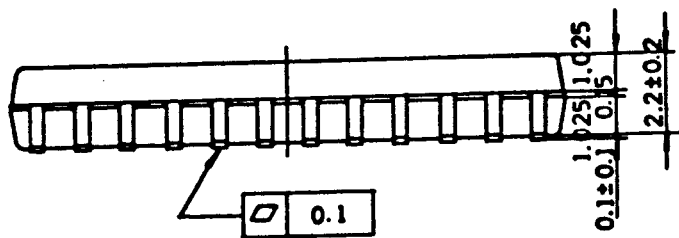
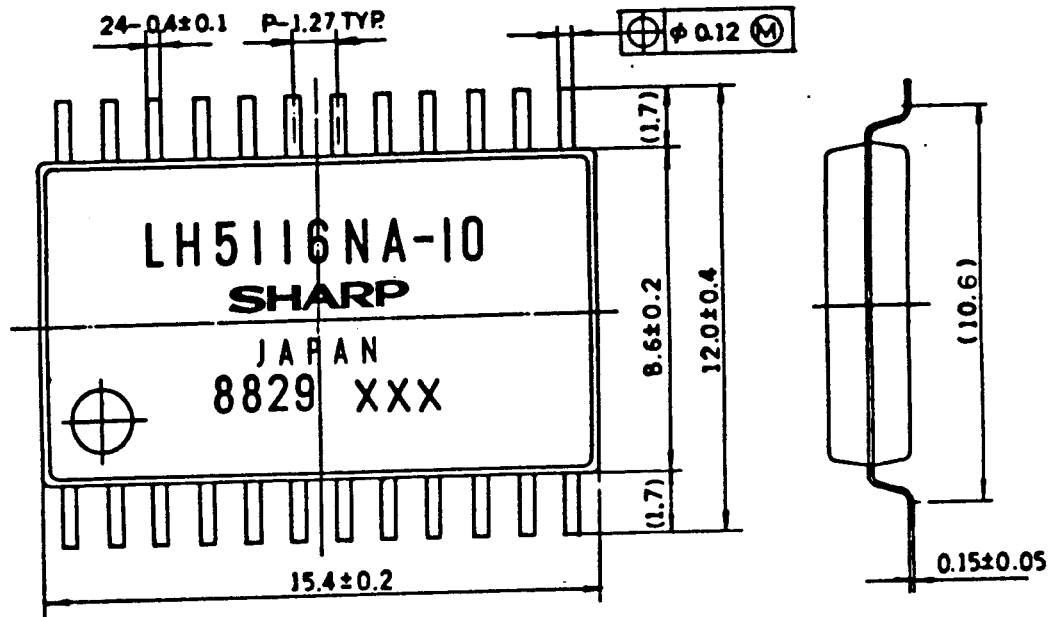
Timing Chart (No.2) [ Note 1 ]



## [NOTE]

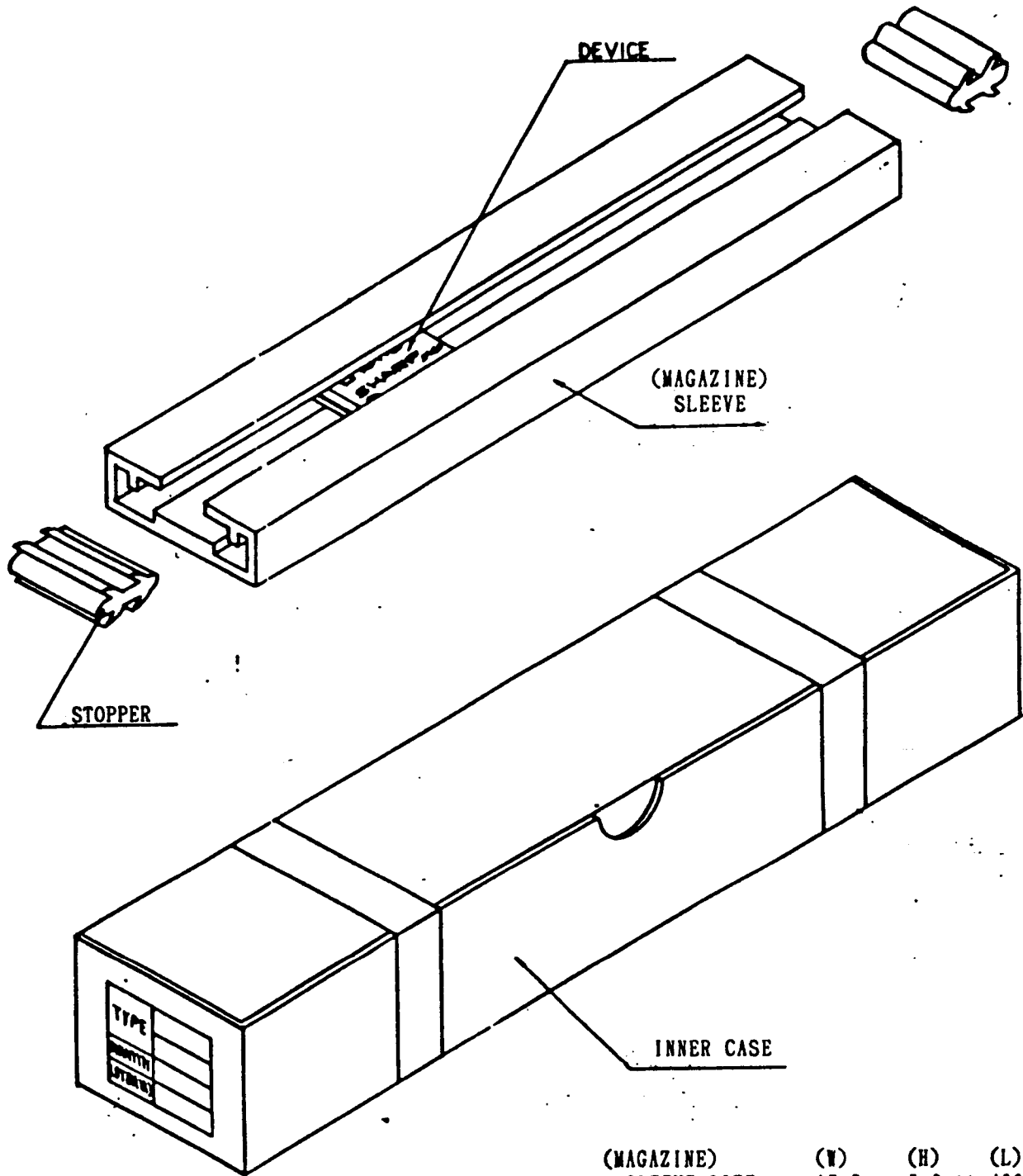
- $\overline{WE}$  must be High when  $A_0 \sim A_{10}$  switch between high and low.
- Write cycle occurs during a overlapping period of  $\overline{CS} = \text{Low}$  and  $\overline{WE} = \text{Low}(t_{wp})$ .
- $t_{wr}$  represents the time interval between the earliest rising edge of  $\overline{CS}$  or  $\overline{WE}$  and the end of write cycle.
- Since during this period, I/O pins assume output state, no input signal 180° out of phase with an output signal is admitted.
- If the rising edge of  $\overline{CS}$  occurs simultaneously with or after the falling edge of  $\overline{WE}$  the output buffer assume high impedance state.
- $\overline{OE}$  must be kept Low level.
- $D_{OUT}$  generates data in phase with input data for the write cycle.
- If both  $\overline{CS}$  remain Low during this period, I/O pins assume output state. At this point, no data input signal 180° out of phase with an output signal.





Plastic body dimensions do not include burr of resin.

適用機種 APPLICABLE MODEL		LH5116NA		尺度 SCALE	5 / 1	單位 UNIT	1 = 1 / 1mm	△			
板厚 THICKNESS		数量 PIECES		材質 MATERIAL		仕上 FINISH		名称 NAME			
						TIN PLATING		SOT24BP			
日付 DATE		'88. 7 . 12		設計 DESIGN		製図 DRAW		校对 CHECK		承認 APPROVE	
				SHARP CORPORATION		IC		コード CODE		AA941-001	
				SHARP CORPORATION				図番 DRAWING No.		AA941-001	



(MAGAZINE) SLEEVE SIZE : (W) 17.5 (H) 5.6 (L) 490  
 CASE SIZE : (W) 80 (H) 62 (L) 510

適用機種 APPLICABLE MODEL		尺規 SCALE		單位 UNIT		△			
LH5116NA		/		1 = 1/1 mm		△			
板厚 THICKNESS		枚数 PIECES		材質 MATERIAL		仕上 FINISH		名 稱 NAME	
								28SOP, 24SOP EXTERNAL APPEARANCE OF PACKING	
日付 DATE		'88. 7 . 12		設計者 DESIGNER		I C 部 長 印		コード CODE	
設計 DESIGN		描圖 DRAW		校核 CHECK		承認 APPROVE		印 號 DRAWING NO.	
SHARP CORPORATION								BJ 2 0 : 0 - 0 1 1 1	

### AC Characteristics Test Conditions

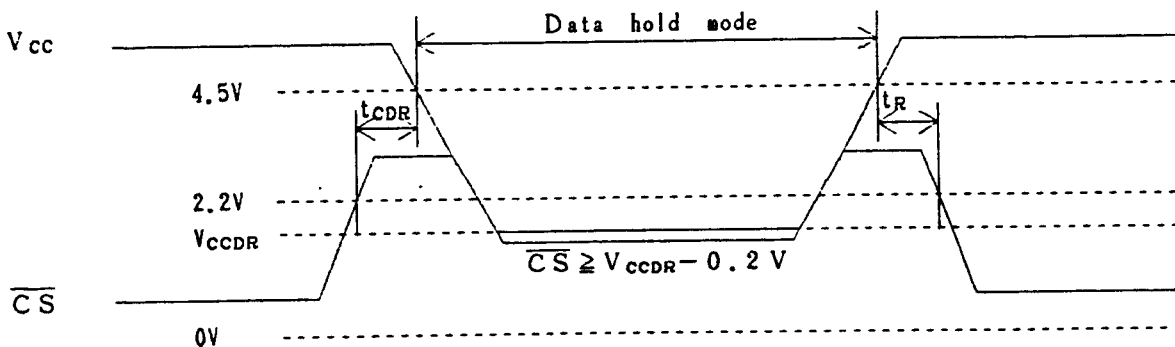
項 目	条 件
Input pulse level	$V_{IN} = 2.2V, V_{IL} = 0.8V$
Input rise and fall time	10 ns
I/O timing reference level	1.5 V
Output load	100 pF + 1 TTL

### 8. Data Hold Characteristics at Low Supply voltage

$T_a = 0 \sim +70^\circ\text{C}$

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data hold supply voltage	$V_{CCDR}$	$\overline{CS} \geq V_{CCDR} - 0.2V$	2.0			V
Data hold supply current	$I_{CCDR}$	$\overline{CS} \geq V_{CCDR} - 0.2V$ $V_{CCDR} = 2V$			1.0 0.2**	$\mu\text{A}$ $\mu\text{A}$
Chip Select Setup time	$t_{CDR}$		0			ns
Chip Select Hold time	$t_R$		$t_{RC}^*$			ns

Note \*Read cycle time \*\*at  $T_a = 25^\circ\text{C}$



### 9. Pin Capacitances

$T_a = 25^\circ\text{C}, f = 1\text{MHz}$

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input capacitance	$C_I$	$V_I = 0V$			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0V$			10	pF

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# SHARP®

## **NORTH AMERICA**

---

SHARP Microelectronics of the Americas  
5700 NW Pacific Rim Blvd.  
Camas, WA 98607, U.S.A.  
Phone: (1) 360-834-2500  
Fax: (1) 360-834-8903  
Fast Info: (1) 800-833-9437  
www.sharpsma.com

## **EUROPE**

---

SHARP Microelectronics Europe  
Division of Sharp Electronics (Europe) GmbH  
Sonninstrasse 3  
20097 Hamburg, Germany  
Phone: (49) 40-2376-2286  
Fax: (49) 40-2376-2232  
www.sharpsme.com

## **JAPAN**

---

SHARP Corporation  
Electronic Components & Devices  
22-22 Nagaike-cho, Abeno-Ku  
Osaka 545-8522, Japan  
Phone: (81) 6-6621-1221  
Fax: (81) 6117-725300/6117-725301  
www.sharp-world.com

## **TAIWAN**

---

SHARP Electronic Components  
(Taiwan) Corporation  
8F-A, No. 16, Sec. 4, Nanking E. Rd.  
Taipei, Taiwan, Republic of China  
Phone: (886) 2-2577-7341  
Fax: (886) 2-2577-7326/2-2577-7328

## **SINGAPORE**

---

SHARP Electronics (Singapore) PTE., Ltd.  
438A, Alexandra Road, #05-01/02  
Alexandra Technopark,  
Singapore 119967  
Phone: (65) 271-3566  
Fax: (65) 271-3855

## **KOREA**

---

SHARP Electronic Components  
(Korea) Corporation  
RM 501 Geosung B/D, 541  
Dohwa-dong, Mapo-ku  
Seoul 121-701, Korea  
Phone: (82) 2-711-5813 ~ 8  
Fax: (82) 2-711-5819

## **CHINA**

---

SHARP Microelectronics of China  
(Shanghai) Co., Ltd.  
28 Xin Jin Qiao Road King Tower 16F  
Pudong Shanghai, 201206 P.R. China  
Phone: (86) 21-5854-7710/21-5834-6056  
Fax: (86) 21-5854-4340/21-5834-6057

### **Head Office:**

No. 360, Bashen Road,  
Xin Development Bldg. 22  
Waigaoqiao Free Trade Zone Shanghai  
200131 P.R. China  
Email: smc@china.global.sharp.co.jp

## **HONG KONG**

---

SHARP-ROXY (Hong Kong) Ltd.  
3rd Business Division,  
17/F, Admiralty Centre, Tower 1  
18 Harcourt Road, Hong Kong  
Phone: (852) 28229311  
Fax: (852) 28660779  
www.sharp.com.hk

### **Shenzhen Representative Office:**

Room 13B1, Tower C,  
Electronics Science & Technology Building  
Shen Nan Zhong Road  
Shenzhen, P.R. China  
Phone: (86) 755-3273731  
Fax: (86) 755-3273735